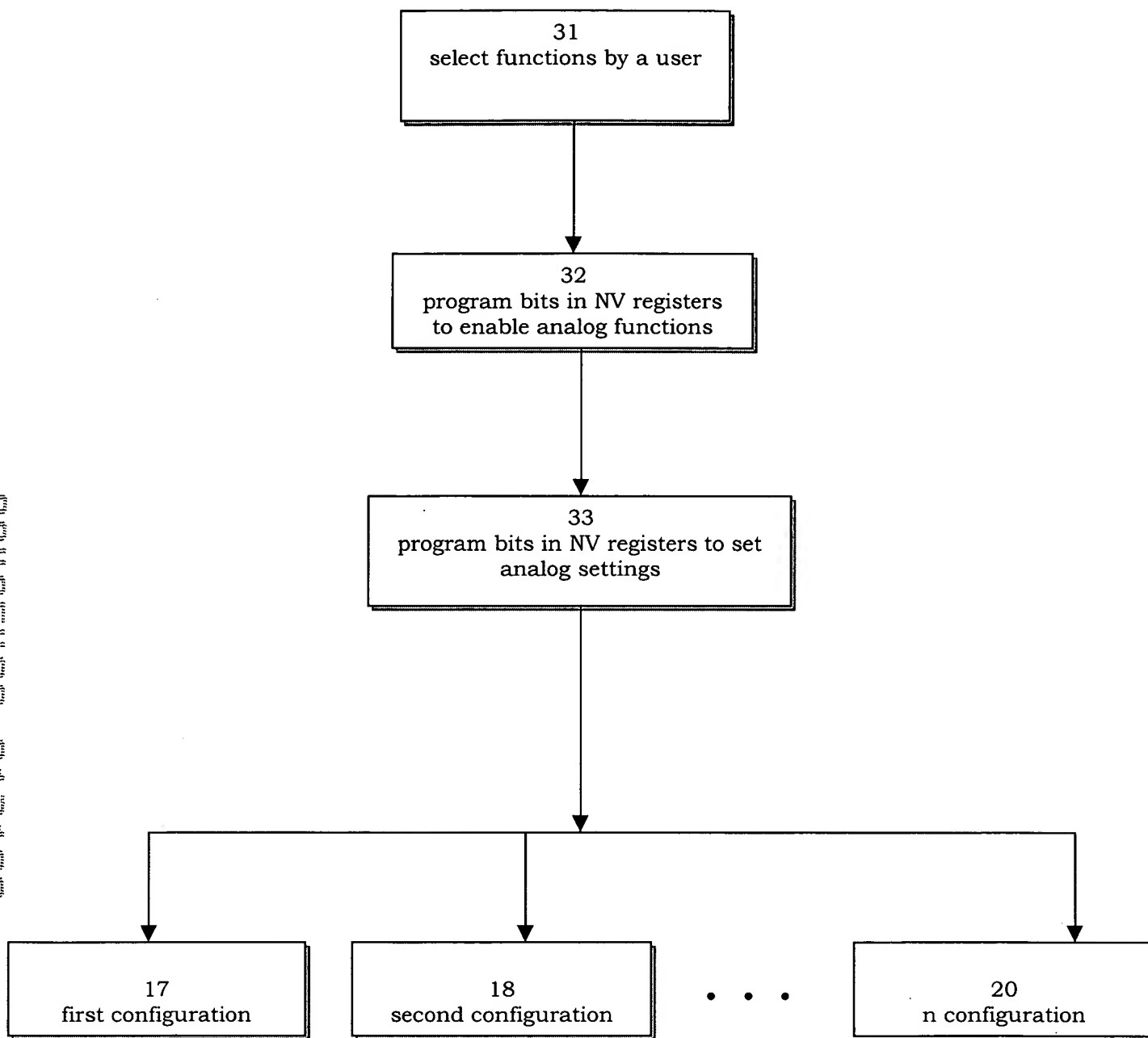


FIGURE 1

FIG. 2 is a flowchart illustrating a method for configuring a device. The method starts with a user selecting functions (31), followed by programming bits in NV registers to enable analog functions (32), and then programming bits in NV registers to set analog settings (33). The process then branches into multiple configurations (17, 18, ..., 20), including the first configuration, second configuration, and n configuration.



*FIGURE 2*

Byte 0

Bits 6-5	Reset timeout	Bits 4-0	Reset range
11	200ms	10000	4.625
10	100ms	01000	4.375
01	50ms	00100	2.9
00	25ms	00010	2.65
		00001	2.15

FIGURE 3A

Byte 1

Bit 6	Complete config write disable	Bit 5	Vsense overvoltage/undervoltage	Bit 4	Responds to all addresses
1	Write disable	1	Undervoltage	1	Respond to all addresses
0	Write enable	0	Overvoltage	0	Respond to pin addresses

Bit 3	Change device identifier code	Bits 2-0	Watchdog interval
1	Respond to 1011	111	6.4s
0	Respond to 1010	110	3.2s
		101	1.6s
		100	.8s
		011	.4s
		00X	off

FIGURE 3B

Byte 2

Bits 7-5	Osc Trim	Bit 4	Full Mem/ Half Mem	Bits 3-0	Bandgap (Vsense) trim
111	Slower	1	4K/16K	1111	Lower
000	Faster	0	2K/8K	0000	Higher

*FIGURE 3C*

Byte 3

Bit 7	Config write disable	Bits 6-4	Full Mem/ Half Mem	Bits 3-0	Vtrip trim
1	Write disable	111	Part 8	1111	Lower
0	Write enable	110	Part 7	0000	Higher
		101	Part 6		
		100	Part5		
		011	Part4		
		010	Part3		
		001	Part2		
		000	Part1		

*FIGURE 3D*

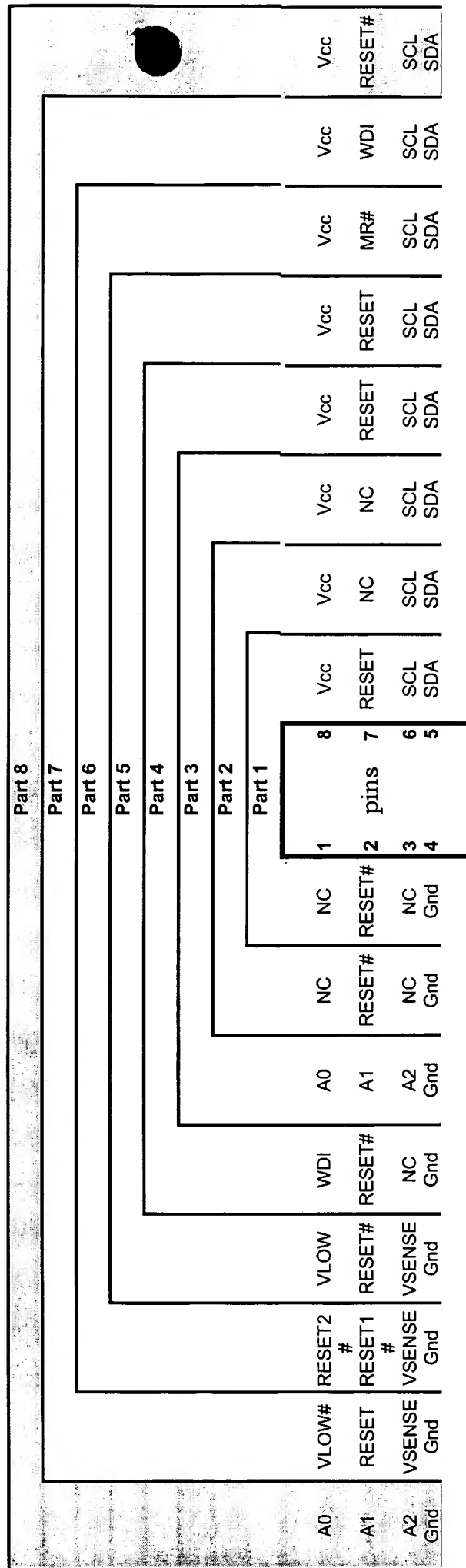


FIGURE 4

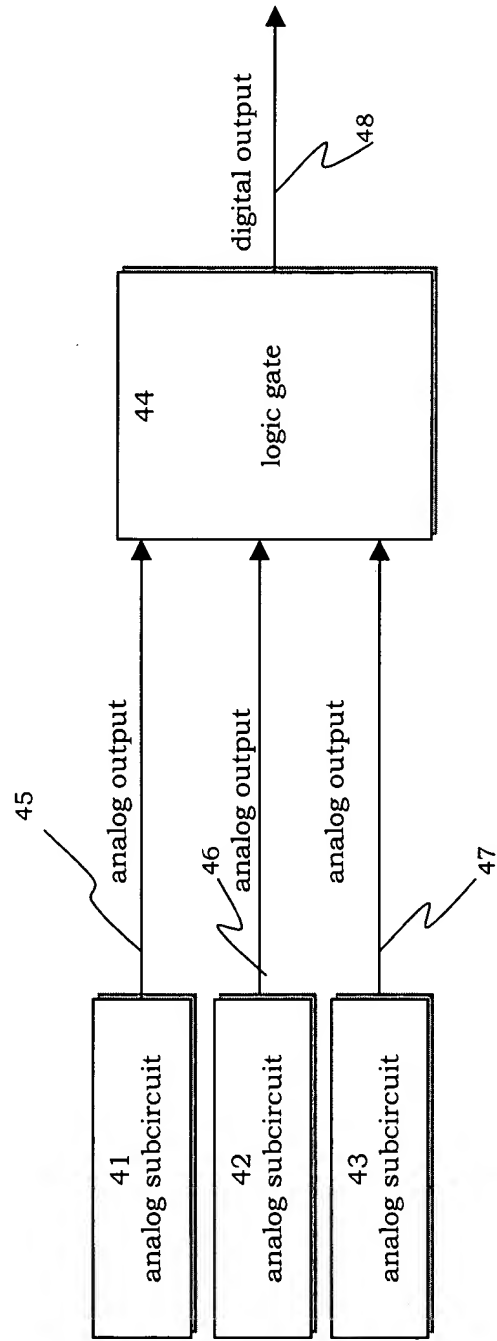


FIGURE 5